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STUDY OF VELOCITY SATURATION AND CARRIER SCATTERING EFFECTS IN TRI-GATE FINFET FOR SOC APPLICATIONS

Rajiv Ranjan Thakur[*1], Pragati Singh[2] & R.K. Singh[3]
[*1,2&3]Dept. of ECE, National Institute of Technology Mizoram

ABSTRACT

In this paper the velocity saturations effects and carrier confinements has been described in accordance with the leading 22nm technology for the multiple gate device. Also, the various short channel effects and their impacts on the device parameters. The subthreshold swing and DIBL was found to be within the acceptable limits and thus the variation in the threshold voltage with respect to the drain voltage and its impact on the device on-state current has been described. The device was simulated using the Sentaurus TCAD and the mathematical operations have been out using MATLAB and Origin Pro.

Keywords: *TG-FinFET, Carrier Velocity Saturation, Carrier Confinements, Subthreshold Swing, DIBL.*

I. INTRODUCTION

Due to the continuous scaling of the MOSFET the traditional MOSFET have reached its fundamental limit and at 22nm technology node its becomes may be difficult for the industry to use the MOSFET due to uncontrolled Short channel effect in the device and thus poor electrostatic control on the channel will degrade the overall device performance [1,2,3]. Thus, we need a device which will offer a better and improved electrostatic control and overall device control over the channel [4]. The idea was to improve the number of gates such that the channel can be controlled from the multiple sides and thus the device that was invented is called as FinFET [5,6].

In this paper, a simulation and numerical study of the Tri-Gate FinFET has been carried out to show its flexibility and advantages for the semiconductor industry. The short channel dependency parameters have been also calculated and a brief discussion has been given on the short channel effects suppression in the said device. Also, the effect of the carrier confinements has been examined along with the velocity saturation effects and high mobility effects to further analyze the device. The device will be applicable to be used in the semiconductor industry as the parameters are found to be in the acceptable limits as per the ITRS reports and also further scaling of the device is possible and will be discussed in our upcoming paper. Also, the device has been studied for maintain its reliability to an increased drain bias at a lower technology node.

II. DEVICE STRUCTURE

The cross-section view of the simulated device is presented in Fig. 1.0 and 1.1 respectively. The degradation model has been used together with a drift-diffusion model to observe the interface trap charges and their density at the interface. Due to the presence of high impurity atom in the active region i.e. channel and considering interface traps at the Oxide Silicon interface Shockley-Read-Hall (SRH) model has been included.

Table.1.0 Parameters used for simulations and calculations

S. No	Parameters	Values
1	Channel Length (Lg)	22 nm
2	Source/Drain Length (Ls or Ld)	30 nm
3	Oxide Thickness (Tox)	1nm
4	Gate Voltage (Vgs)	0.8 V
5	Acceptor Doing Concentration (Na)	10^{18} cm^{-3}

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6	Donor Doping Concentration ·(Nd)	10^{20} cm^{-3}
7	Work function (ﻗms)	4.4 eV

Considering retrograde and uniform doping concentrations for better results, Band Gap Narrowing (BGN) and Auger Recombination models are included in the simulations. The effects of scattering were studied using the multi-valley model which provide us a way to visualize the scattering in the channel. The low high doping profile in the channel help us to suppress the scattering effect which stops the formation of Hot Carrier in the channel and hot carrier effect will be prevented in the device various short channel effect in the channel.

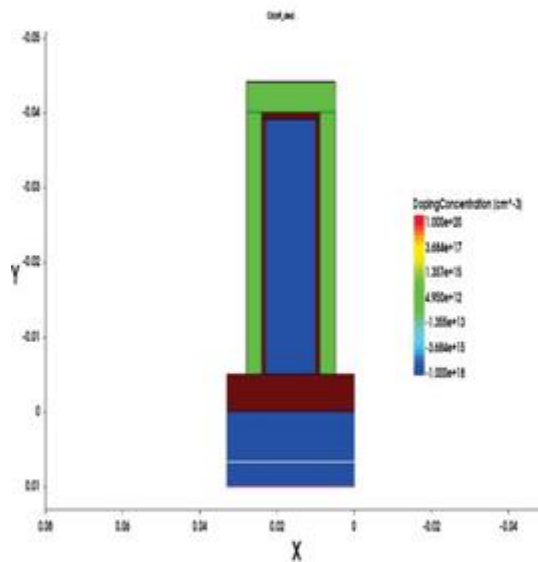

Fig.1.0 D cross-section of the simulated device

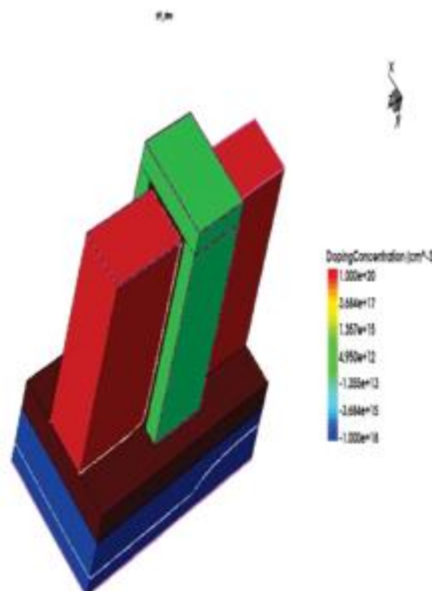

Fig.1.1 3D cross-section of the simulated device

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Further, density gradient quantization model has been used to further study the quantization that took place near the channel region of the device. This also helps us to understand the carrier confinements and well formation in the device.

III. RESULTS AND DISCUSSIONS

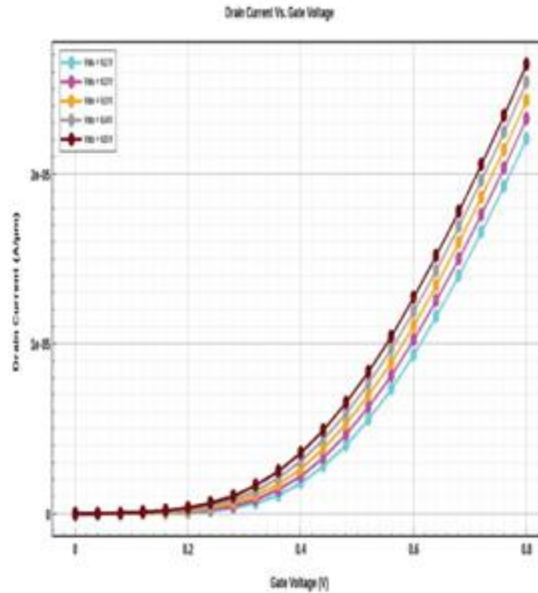

Fig.2.0 Drain Current Vs. Gate Voltage for Simulated Device

The Variations of Drain Current as a function of the drain voltage has been plotted in Fig. 2.0. It was observed that the device offers an on-off ratio of 10^8 with an on current 2.2 x 10^{-5} A/μ m of and off current of 8.35 x 10^{-13} A/ μm. The device was also found to have a steep subthreshold swing of 73.22 mV/Dec and suppressed DIBL of 52.25 mV/V. These values are within the acceptable limit for these parameters and values of SS clearly indicates that the device can be turned off very easily without much difficulties which leads to lower Sub-Threshold Conduction. Further, the value of DIBL also indicates that the values of the threshold voltage will not be much affected as the drain bias is being increased to increase the on currents.

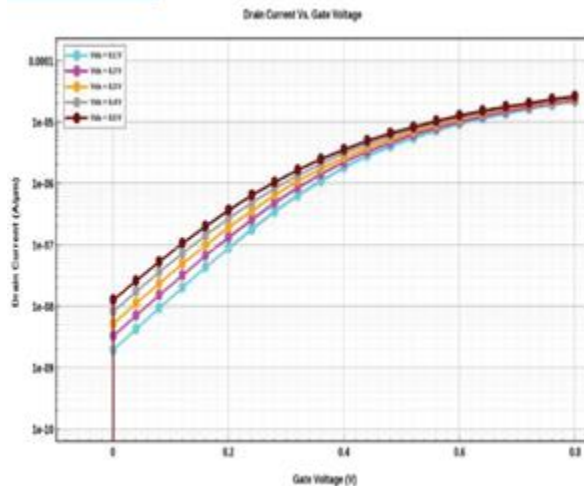

Fig.2.1 Log Drain Current Vs. Gate Voltage for Simulated Device

The variation of the Drain Current as a function of gate to source bias has been plotted in the fig 2.1. it is clear from the plot that the device has an excellent channel control and thus an improved device parameter and suppressed short channel effects.

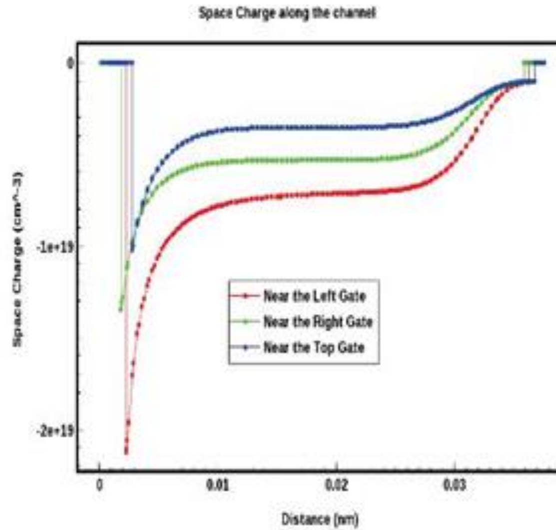

Fig.2.2 Space Charge variations along the channel

The variations of Space Charge along the channel have been plotted in Fig.2.7. It is clear from the obtained plot the Space Charge is maximum near the top gate. The space charge was somehow stable near the two gates of the device and was found to be decreasing in the center as we move towards the drain end of the device.

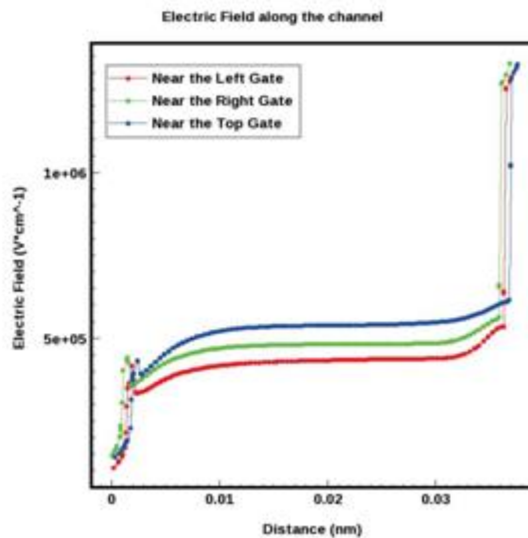

Fig.2.3 Electric Field variations along the channel

The variations of Electric Field along the channel have been plotted in Fig.2.3. It is clear from the obtained plot the Electric Filed is maximum near the top gate. The electric field was somehow stable near the two gates of the device and was found to be decreasing in the center as we move towards the drain end of the device.

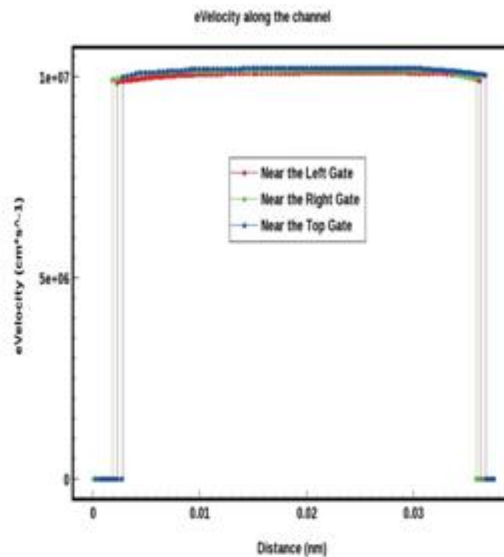

Fig.2.4 Electron Velocity variations along the channel

The variation of electron velocity has been plotted in Fig.2.4 along the channel. The velocity of the electrons was found to in the acceptable limits and thus we have an improved mobility effects in the channel thus no carrier scattering effect in the device.

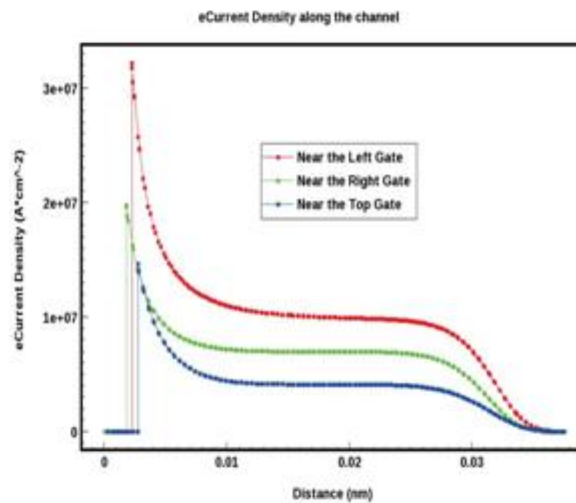

Fig.2.5 Electron Density variations along the channel

The variations of Electron current density of the simulated device have been depicted in Fig. 2.5. The density of electrons was maximum at the left gate followed by right gate and top gate. This clearly depicts that as the bias is being more positive at the gate the number of electrons near the interface increases as compared to the mid-point of the channel and thus as the bias will be increased these electrons will be confined in a particular direction for movements from source to the drain without much scattering and we will achieve an increased drain current as compared to the traditional MOSFET device with a single gate. Further, as the electric field is being applied from both the gates it is easier for the carrier to move towards the channel under the controlled environment.

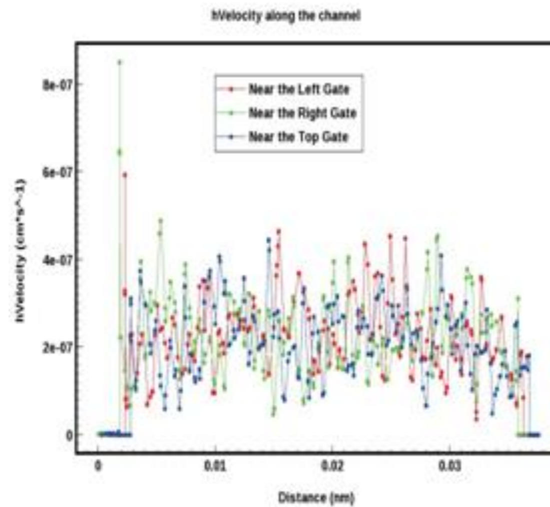

Fig.2.6 Electric Field variations along the channel

The variations of the hole velocity have been plotted along the channel for the simulated device in Fig.2.6. The hole velocity was found to be very low and thus there will not be a formation n of hot carriers in the channel thus no hot carrier effects.

IV. CONCLUSION

In this paper, we have studied the characteristics and performance of the Tri-Gate FinFET in Nano regimes for SoC applications. It was found that the control mechanism was improved due to multiple side control and thus the short channel effect has been suppressed. The effects of the scaling down the technology node to improve the device performance has been examined and discussed briefly based on the simulations results. The study also describes the reasons for the decrease in the threshold voltage with respect to the Drain to Source voltage.

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